ABSTRACT OF THE DISCLOSURE

In order to achieve a processor that does not require processing time for branching processing and is ensured the flexibility of the processing content, an adder adds a start address stored in start address parts and selected by a selector and a stored content (relative address) of a program counter to output a current execution instruction address. An execution unit executes an instruction of the address of a program storing part. A comparator compares the address with an end address stored in end address storing parts and selected by a selector. When the addresses are matched, the selectors are switched, and the program counter is reset, so that branching can be performed without requiring an instruction cycle. The start address storing parts are rewritten by a supervisory processor, where appropriate.